A Novel Low Voltage Current Compensated High Performance Current Mirror/NIC

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Abstract

In this paper a novel high output impedance, low input impedance, wide bandwidth, very simple mirror/source structure with input and output voltage requirements less than that of a simple current mirror is presented. It can be also used as variable negative impedance converter (variable-NIC) by modifying amplifier transistors' aspect ratios. The circuit's principle of operation is discussed and compared to simple and low voltage cascode (LVC) current mirrors. Working with power supplies less than 1volt, the proposed circuit provides output impedance greater than LVC current mirror. Such outstanding features of this current mirror as high output impedance~25.3M, low input impedance~44, wide bandwidth~498MHz, low input voltage ~ 415mV, low output voltage ~ 149mV and low current transfer error ~1.3% (all at 10μA) makes it an outstanding choice for high performance applications. Simulation results in BSIM 0.35μm CMOS technology with Hspice are given in comparison with simple, and LVC current mirrors to verify and validate the performance of the proposed current mirror/NIC.

Keywords

NIC, Current mirror, Low voltage, high output impedance, low input impedance, and high frequency.

1. Introduction

Current mirror is one of the most essential building blocks in analog integrated circuits which its performance affects qualitive performance of the system. The major draw backs of conventional current mirrors due to technology scaling trend in VLSI design tend to be: voltage supply reduction requirement, input and output impedances degradation, and high frequency malfunctioning. Considering that in many applications, the performance of the traditional current mirrors are inadequate; many researches are reported improving the current mirrors' performance [1]-[13]. Traditional current mirrors/sources, such as simple, cascode, and regulated current mirrors/sources [1], suffer from a trade-off between the output resistance and the compliance voltage (the minimum voltage required for the current mirror/source to operate). Some topologies such as the high swing cascode [2] and the active regulated cascode [3] have improved Rout with a relatively low compliance voltage of 2VDSsat. This, however, may still be too large to be tolerated in low voltage circuits. In [4]-[5] are presented current sources with high output resistance and compliance voltage of one V_{DSsat}. The circuit in [4] works based on sensing the voltage across the current source. Its draw backs are high frequency degradation and instability problems. The circuit in [5] uses positive feedback to increase its output impedance reduce its output compliance voltage. These circuits however are used as current sources and are not suitable as current mirrors. Although the circuits proposed in [6]-[8] eliminate some of the above mentioned draw backs, however they suffer from heavy structures and large chip area consumption. In order to further relaxing voltage requirements some techniques such as body driven topologies are introduced in literatures [9]-[11]. These circuits suffer from lower bandwidth, expensive technology and higher input impedance due to g_{mb} being lower than gm.

In this work a high performance current mirror is presented in which favorably most of aforementioned characteristics are improved.

In section II the proposed current mirror is explained. Section III includes the results achieved from simulations. And finally Section IV concludes this paper.

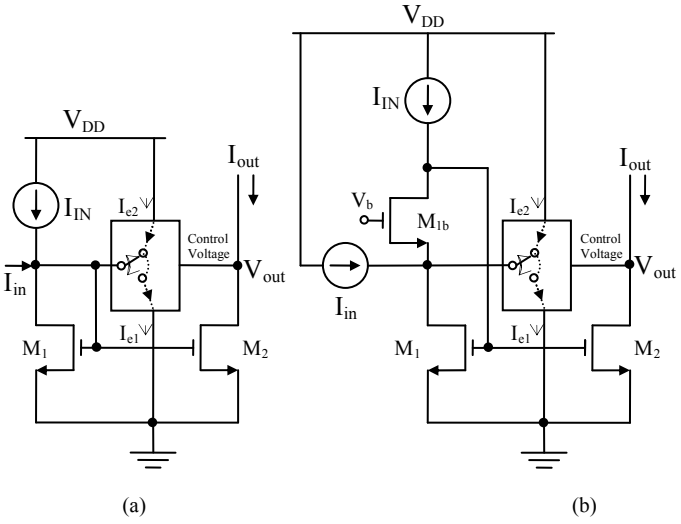

Figure 1: (a) A conceptual schematic of the low-voltage current mirror/source (b) improved version of (a).

2. Proposed high performance current compensated current mirror

2.1. Principle of Operation

Figure1 shows the conceptual schematic of the proposed current mirror/source. The Ie1 and Ie2 error currents are controlled by V_{out}. When V_{out} approaches VDD then Ie1 is increased and thus current flowing through M1 is decreased. This will decrease the output current so that it will remain constant for high output voltages, implying that the output

impedance is increased. The result is an output impedance for the proposed current mirror much more than that of the traditional one. When V_{out} approaches GND then Ie2 increases making the current flowing through M1 to increase as well. This will increase the output current in a way that it will remain constant for lower output voltages. Interestingly, this phenomenon is true at voltages even smaller than V_{DSsat} which is the operation extreme of simple current mirror. So the proposed circuit is favorably well suited for works at low voltage systems.

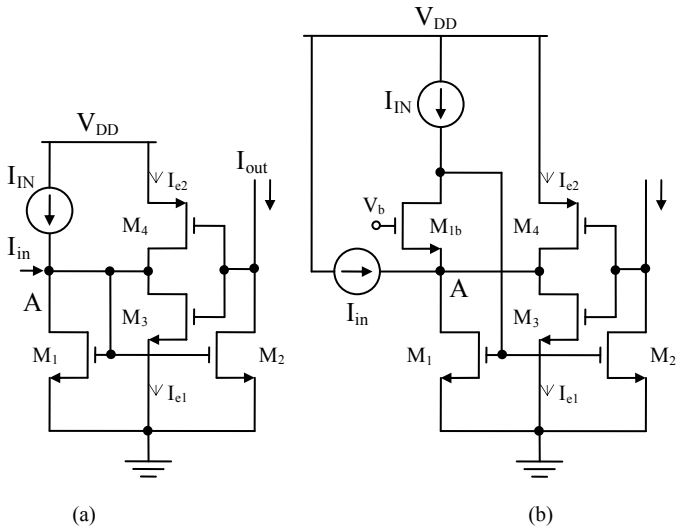

Figure 2: (a) the proposed current mirror (b) improved version of (a).

2.2. Circuit Analysis

Current mirror's output voltage can vary from zero to V_{DD} due to either output current variations (when it is used as signal path) or voltage bias variations proportional to common mode voltage of differential amplifier when it is used as a tail. This variation affects output transistor's current by channel length modulation. To achieve high performance current mirrors these (output current) variations must be eliminated. To do this, many methods are proposed so far each suffering some drawbacks while introducing some benefits. Figure 2 (a) shows the proposed current compensated current mirror which efficiently and simply eliminates the problem.

When the output voltage is increased, the channel length modulation effect tends to increase the output current. Meanwhile as a result of V_{GS3} increment, transistor M_3 draws an error current from input node, making the M_1 current to be decreased. By adjustment of the error current very high output impedances even higher than that of cascode current mirror can be achieved, while its output headroom becomes even more than that of a simple current mirror.

There is no restriction for transistors M_3 and M_4 to work in saturation region. In fact, they can work in saturation, triode, and even off regions. This is an interesting result, firstly because the voltages of the circuit are not limited by addition of these transistors, secondly power consumption is not increased that much because:

1- One of transistors is off while the small error current flows through the other one.

2- The aspect ratios of M_3 and M_4 transistors are adjusted for minimum quiescent current when they operate under saturation conditions.

In Figure 2 (a) the value of one V_{gs} used for input transistor does not satisfy well the low voltage applications. Favorably a useful structure is proposed to overcome this need one of which is shown in Figure 2 (b). I_{IN} defines bias point and I_{in} acts as input signal.\

2.2.1. Low voltage analysis

When output voltage becomes lower than $V_{DS(sat)}$, M_2 will enter the triode region and output current will decrease tremendously. In this condition M_3 enters cut-off and its output resistance increases tremendously while M_4 becomes strongly inverted and introduces an extra current to the input node (node 'A') which increases the V_{GS1} voltage. As the result of increased V_{GS1}, the output current will be compensated to a useful level even at lower output voltages. This implies that circuit is capable of operation in even lower voltages than that of simple current mirror.

For low voltage operation at input node, FVF structure is adopted [12]. This structure makes the circuit to operate at input voltages as low as possible for V_{Dsat}. It also reduces the input impedance and increases the output impedance.

2.2.2. Output impedance analysis

Figure 3 shows the equivalent circuit for output impedance calculation. When output voltage increases, because of channel length modulation an extra current is drawn from output. This is interpreted as finite output impedance. In this condition, M3 current increases and M4 current decreases and as a result the proposed amplifier draws an error current from the input node (node A) which decreases the VGS1. As the result of decreased VGS1, increased output current will be compensated so that the output current maintains its previous level, even at higher output voltages.

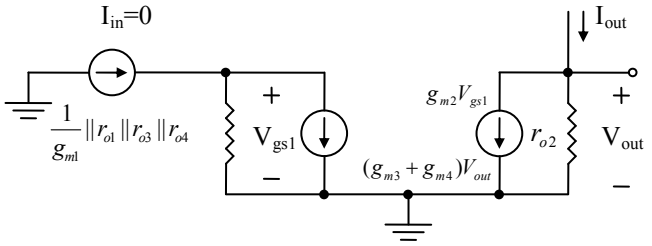

Figure 3: Equivalent circuit of proposed current mirror for Ro calculation.

This implies that output impedance of the circuit is increased better than traditional current mirrors. This capability becomes much more interested when considering that the circuit has the same high band width of the simple current mirror.

This function of the proposed circuit can be taken as output impedances from very high to negative values according to following equations.

a) The proposed current mirror (Fig 2-a)

$$V_{gs1}=-(g_{m3}+g_{m4})\times V_{out}\times\left[\frac{1}{g_{m1}}\|r_{o1}\|r_{o3}\|r_{o4}\right] \quad (1)$$

$$V_{out}=r_{o2}\times(I_{out}-g_{m2}\times V_{gs1})$$

$$=r_{o2}\times I_{out}+r_{o2}\times g_{m2}\times(g_{m3}+g_{m4})\times V_{out}\times\left[\frac{1}{g_{m1}}\|r_{o1}\|r_{o3}\|r_{o4}\right] \quad (2)$$

$$V_{out}\left[1-r_{o2}\times g_{m2}\times(g_{m3}+g_{m4})\times\left[\frac{1}{g_{m1}}\|r_{o1}\|r_{o3}\|r_{o4}\right]\right]=r_{o2}\times I_{out} \quad (3)$$

$$R_{out}=\frac{V_{out}}{I_{out}}=\frac{r_{o2}}{1-r_{o2}\times g_{m2}\times(g_{m3}+g_{m4})\times\left[\frac{1}{g_{m1}}\|r_{o1}\|r_{o3}\|r_{o4}\right]} \quad (4)$$

From (4) it can be concluded that:

$$if\ \ 1-r_{o2}\times g_{m2}\times(g_{m3}+g_{m4})\times\left[\frac{1}{g_{m1}}\|r_{o1}\|r_{o3}\|r_{o4}\right]=0\Rightarrow R_{out}=\infty$$

$$if\ \ 1-r_{o2}\times g_{m2}\times(g_{m3}+g_{m4})\times\left[\frac{1}{g_{m1}}\|r_{o1}\|r_{o3}\|r_{o4}\right]>0\Rightarrow R_{out}>0$$

$$if\ \ 1-r_{o2}\times g_{m2}\times(g_{m3}+g_{m4})\times\left[\frac{1}{g_{m1}}\|r_{o1}\|r_{o3}\|r_{o4}\right]<0\Rightarrow R_{out}<0$$

Since $\frac{1}{g_{m1}}\|r_{o1}\|r_{o3}\|r_{o4}\cong\frac{1}{g_{m1}}$ and $g_{m1}\cong g_{m2}$ then $R_{out}=\infty$ will be true if $r_{o2}\times(g_{m3}+g_{m4})=1$, the condition that can be satisfied by adjusting $\frac{W_3}{L_3}$ and $\frac{W_4}{L_4}$ to small values.

b) Improved version of the proposed current mirror (Fig 2-b)

$$V_{ds1}=-(g_{m3}+g_{m4})\times V_{out}\times\left[\frac{1}{A\times g_{m1}}\|r_{o1}\|r_{o3}\|r_{o4}\right],\ A=1+g_{m1b}r_{o1b} \quad (5)$$

$$V_{out}=r_{o2}\times(I_{out}-g_{m2}\times V_{gs1})=r_{o2}\times(I_{out}-g_{m2}\times A\times V_{ds1})$$

$$=r_{o2}\times I_{out}+r_{o2}\times g_{m2}\times A\times(g_{m3}+g_{m4})\times V_{out}\times\left[\frac{1}{A\times g_{m1}}\|r_{o1}\|r_{o3}\|r_{o4}\right] \quad (6)$$

$$V_{out}\left[1-r_{o2}\times g_{m2}\times A\times(g_{m3}+g_{m4})\times\left[\frac{1}{A\times g_{m1}}\|r_{o1}\|r_{o3}\|r_{o4}\right]\right]=r_{o2}\times I_{out} \quad (7)$$

$$R_{out}=\frac{V_{out}}{I_{out}}=\frac{r_{o2}}{1-r_{o2}\times g_{m2}\times A\times(g_{m3}+g_{m4})\times\left[\frac{1}{A\times g_{m1}}\|r_{o1}\|r_{o3}\|r_{o4}\right]} \quad (8)$$

2.2.3. Frequency response analysis

The proposed current mirror (Fig 2-a)

$$C_{in}=C_{ds1}+C_{gs1}+C_{ds3}+C_{ds4}+C_{gs2}+C_{gd2}+C_{gd3}+C_{gd4} \quad (9)$$

$$V_{in}=\frac{I_{in}}{g_{ds1}+g_{ds3}+g_{ds4}+g_{m1}+C_{in}S} \quad (10)$$

$$I_{out}+V_{in}S(C_{gd3}+C_{gd4}+C_{gd2})=g_{m2}V_{in} \quad (11)$$

$$I_{out}=V_{in}\left[g_{m2}-S(C_{gd3}+C_{gd4}+C_{gd2})\right] \quad (12)$$

$$\frac{I_{out}}{I_{in}}=\frac{g_{m2}-S(C_{gd3}+C_{gd4}+C_{gd2})}{g_{ds1}+g_{ds3}+g_{ds4}+g_{m1}+C_{in}S} \quad (13)$$

b) Improved version of the proposed current mirror (Fig 2-b)

$$C_{in}=C_{ds1}+C_{ds3}+C_{ds4}+C_{gd3}+C_{gd4}+C_{gs1b} \quad (14)$$

$$C_{g1}=C_{gs1}+C_{gs2}+C_{gd2} \quad (15)$$

$$I_{out}=(g_{m2}-SC_{gd2})V_{g1}-S(C_{gd3}+C_{gd4})V_{in} \quad (16)$$

$$I_{in}=(g_{ds1}+g_{ds3}+g_{ds4}-SC_{in})V_{in}+g_{m1}V_{g1} \quad (17)$$

Where:

$$v_{g1}=\left(1+\frac{g_{m1b}}{g_{ds1b}+S(C_{ds1b}+C_{gd1})}\right)V_{in} \quad (18)$$

Substituting (18) into (16) and (17) gives:

$$\frac{I_{out}}{V_{in}}=(g_{m2}-SC_{gd2})\left(1+\frac{g_{m1b}}{g_{ds1b}+S(C_{ds1b}+C_{gd1})}\right)-S(C_{gd3}+C_{gd4}) \quad (19)$$

And

$$\frac{I_{in}}{V_{in}}=(g_{ds1}+g_{ds3}+g_{ds4}-SC_{in})+g_{m1}\left(1+\frac{g_{m1b}}{g_{ds1b}+S(C_{ds1b}+C_{gd1})}\right) \quad (20)$$

Dividing (19) by (20) gives:

$$\frac{I_{out}}{I_{in}}=\frac{g_{m1b}g_{m2}-Sg_{m1b}C_{gd2}-S^2(C_{gd3}+C_{gd4})(C_{gd1}+C_{ds1b})}{g_{m1b}g_{m1}+Sg_{m1}(C_{ds1b}+C_{gd1})+S^2C_{in}(C_{ds1b}+C_{gd1})} \quad (21)$$

Which can be simplified as:

$$\frac{I_{out}}{I_{in}}=\frac{g_{m2}\left(1-\frac{C_{gd2}}{g_{m2}}S\right)\left(1+\frac{(C_{gd3}+C_{gd4})(C_{gd1}+C_{ds1b})}{g_{m1b}C_{gd2}}S\right)}{g_{m1}\left(1+\frac{C_{in}}{g_{m1}}S\right)\left(1+\frac{C_{ds1b}+C_{gd1}}{g_{m1b}}S\right)} \quad (22)$$

3. Simulation Results

HSPICE simulation of the proposed current mirror is carried out in a BSIM 0.35µm CMOS process. To investigate the performance improvement (especially, input and output impedance, input and output voltage swing, power and band width) of the proposed current mirror compared to simple and LVC current mirrors, their simulation results are compared.

Referring to Figure 2 the effect of I_{e1} and I_{e2} on V_{GS1} is shown in Figure 4 (a). It can be seen that for a fixed input current by output voltage variations, V_{GS1} of simple current mirror is a constant value, while for proposed current mirror V_{GS1} varies. This VGS1 variation adjusts the output current to the desired values yielding high impedance and low voltage operation. Figure 4 (b) shows the I_{e1} and I_{e2} and their effect on output current (I_{out}) when sweeping output voltage (V_{out}) from zero to VDD.

The comparative simulation results are given in Figure 5 for simple, LVC and proposed circuits. In this figure I_{out} is shown in terms of V_{out} sweep. It can be seen that the proposed circuits offer higher output impedances and benefit from lower voltage operation capability.

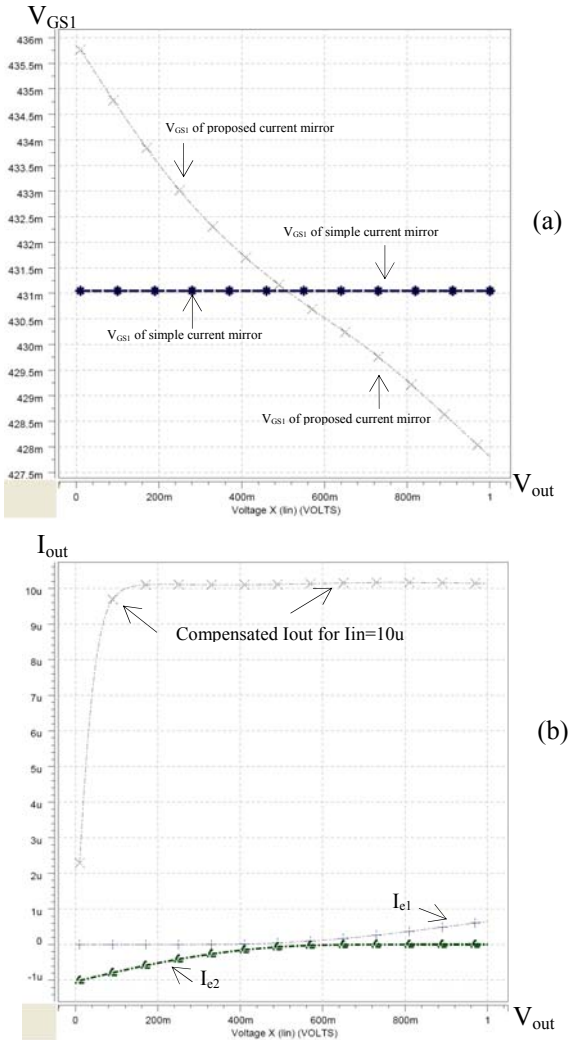

Figure 4: (a) Effect of error current on Vgs1 (b) Ie1 and Ie2 and their effect on Iout

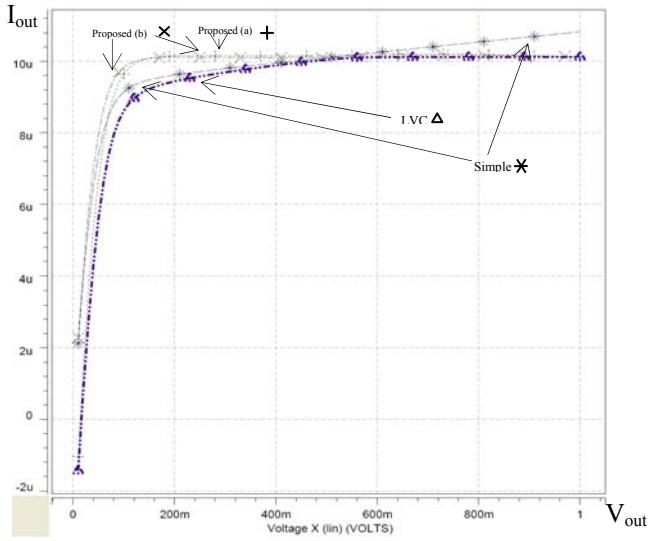

Figure 5: comparative simulation results for simple, LVC and proposed circuits

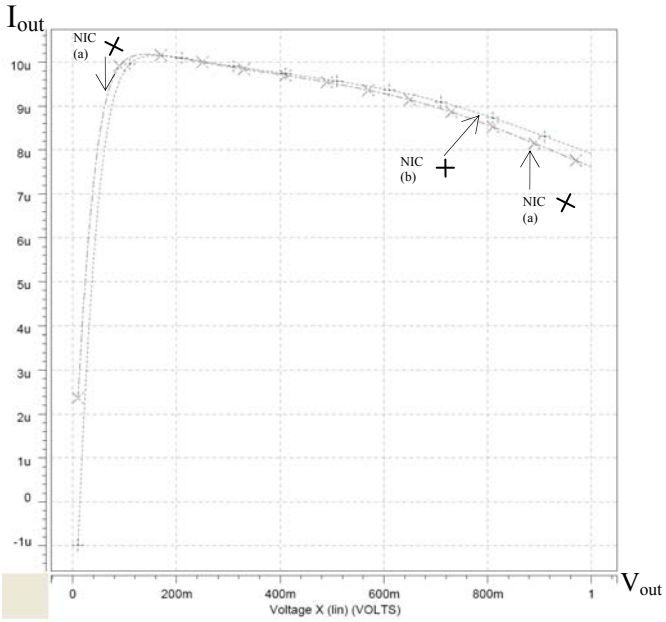

Figure 6: NIC performance of the proposed circuits

Figure 6 shows the simulation results for NIC performance of the proposed circuits. The amount of negative resistance can be varied by adjusting transistor's (M_3) aspect ratios.

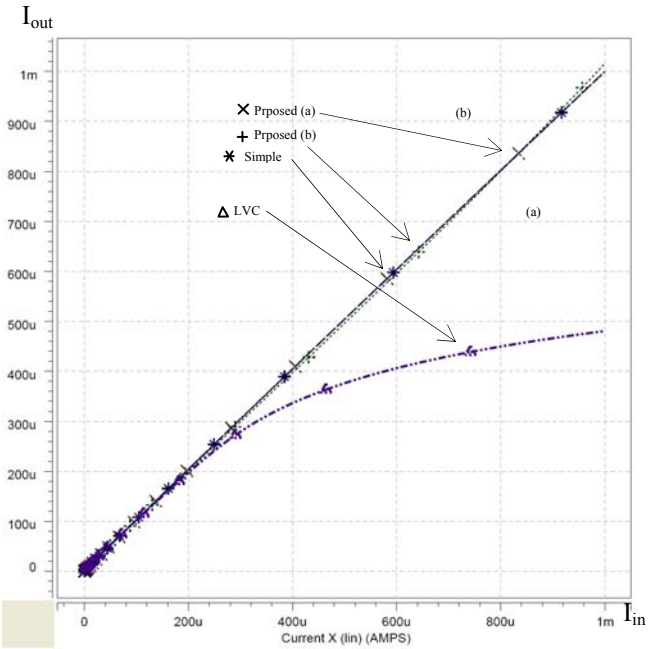

Figure 7: output current dynamic range

Figure 7 shows the output current dynamic range.

Figure 8 compares the input resistance of simple, LVC, and proposed current mirrors.

Figure 9 shows the band width of simple, LVC, and proposed current mirror (R_L=10K and C_L=20pF). It is seen

that the proposed current mirrors have the high band width of the simple current mirror.

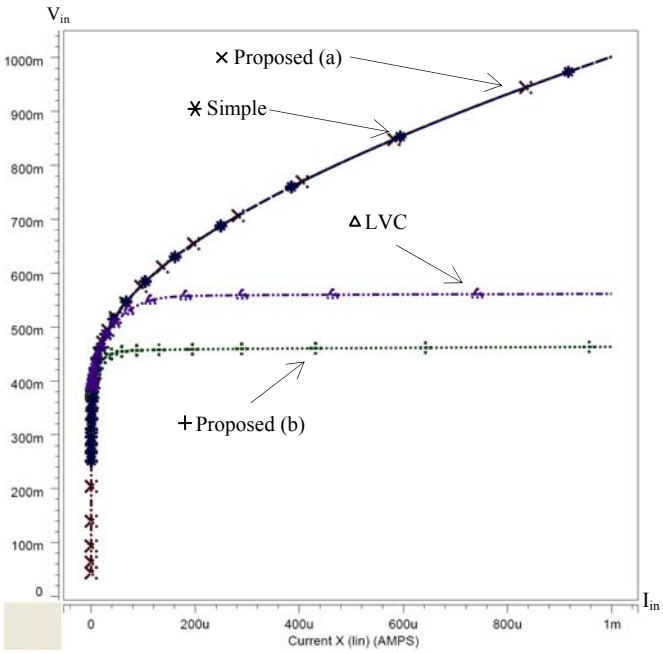

Figure 8 the input resistance of simple, LVC, and proposed current mirrors.

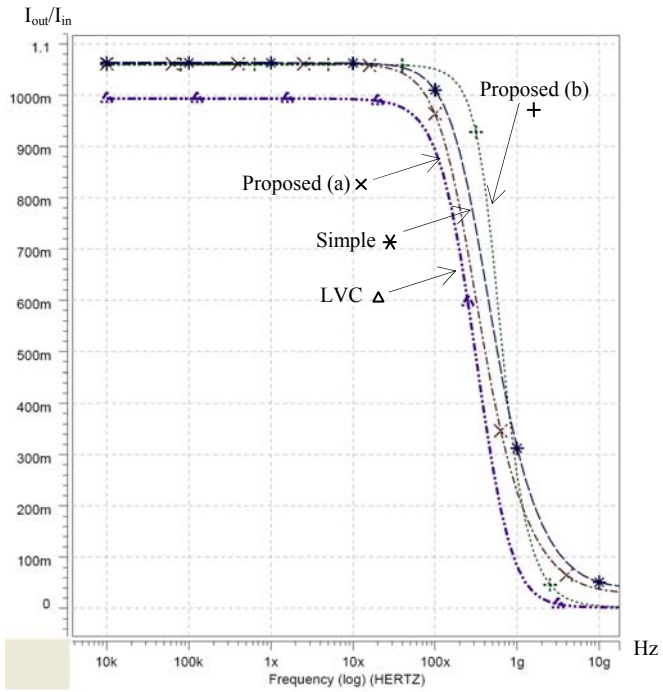

Figure 9: Comparing band width of simple, LVC, and proposed current mirror

The transistors' aspect ratios are given at Table 1. For proposed circuit, transistors' aspect ratios for both current mirror (CM) and NIC operation is available.

Table .1 Transistors aspect ratio

Trans.	Sim.	LVC	Prop. (a)		Prop. (b)	
			CM	NIC	CM	NIC
M1-M2	14/.7	14/.7	14/.7	14/.7	14/.7	14/.7
M3	NA	14/.7	.35/35	8.75/.35	.35/23.8	8.75/.35
M4	NA	14/.7	.35/5.6	2.8/.35	.35/4.2	2.45/.35
M1b	NA	NA	NA	NA	3.5/.35	3.5/.35

Comparative results of proposed current mirrors with some other works are presented at Table 2.

Table .2 comparative results

Ref.	Simple	LVC	[9]	[11]	Prop.(a)	Prop.(b)
I_{IN} (µA)	10	10	12	30	10	10
Offset (µA)	0.83	4.12	8.8	18	0.13	1
Vin(mV)	430	441	NA	300	427	415
Rin(Ω)	580	120	0.02	NA	580	44
Vout(mV)	150	566	1.4	200	168	149
Rout(MΩ)	0.633	22	360	NA	22.2	25.3
P(µW)	21	29	2300	NA	20	28
BW(MHz)	347	196	0.083	2	247	498
Supply (V)	1	1	1	1.5	1	1
Tech.	BSIM 0.35µm	BSIM 0.35µm	90-nm CMOS	TSMC *0.25Jlm* 2P4M	BSIM 0.35µm	BSIM 0.35µm

4. Conclusion

In this work a high performance current mirror is presented with such favorable characteristics as: high output impedance~25.3M, low input impedance~44, wide bandwidth~498MHz, low input voltage ~ 415mV, low output voltage ~ 149mV and low current transfer error ~ 1.3% (all at 10µA). Its simulation results in BSIM 0.35µm CMOS technology with HSPICE are given in comparison with those of simple, and LVC current mirrors to verify and validate the performance of the proposed current mirror/NIC.

The proposed current compensated current mirror (CCCM) shows output impedance greater than traditional cascode current mirrors, while maintaining the output voltage requirement and high bandwidth of the simple current mirror. This circuit's bandwidth, input and output voltage requirements are comparable to those of the simple current mirror. The circuit can show a minimum output voltage even lower than that of the simple current mirror. The proposed current mirror is an outstanding choice for high frequency low power low voltage applications.

9. References

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